Customer No. 22,852
Attorney Docket No.: **04329.3150**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Mie MATSUO et al.	)	Group Art Unit: **Not Yet Assigned**
	)	
Serial No.: **Not Yet Assigned**	)	Examiner: **Not Yet Assigned**
	)	
Filed: **September 30, 2003**	)	
	)	
For: **STACKED TYPE SEMICONDUCTOR DEVICE**	)	
	)	

MAIL STOP PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. With exception of the U.S. patents, copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form. This Information Disclosure Statement is being filed with the above-referenced application.

The following are listed on the accompanying PTO-1449 and are in a non-English language:

1. Japanese Patent Publication No. 2002-110865- discloses an electrical component of a silicon interposer which includes an active element such as a repeater or booster.

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2. Japanese Patent Publication No. 2001-102479 - discloses a silicon interposer of the function which has an interconnection (signal line and ground line).

3. Japanese Patent No. 2760188 (Japanese Patent Publication No. 05-136331) – discloses a multi-chip semiconductor device. The relevance of this document is also discussed at page 2 of the present application.

4. Japanese Patent Publication No. 2000-349229 – discloses a multi-chip semiconductor device. The relevance of this document is also discussed at page 3 of the present application.

5. Japanese Patent Publication No. 05-283606 - discloses a multi-chip semiconductor device. The relevance of this document is also discussed at page 3 of the present application.

Also, an English-language abstract of each document is enclosed.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

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If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: September 30, 2003

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OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	**04329.3150**	Serial No.	**N t Yet Assigned**
Applicants	**Mie MATSUO** et al.		
Filing Date	**September 30, 2003**	Group:	**Not Yet Assigned**

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,624,506 B2	09/23/03	SASAKI et al.			
		6,614,106 B2	09/02/03	MATSUO et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2002-110865	04/12/02	JAPAN			ABSTRACT
		2001-102479	04/13/01	JAPAN			ABSTRACT
		2760188	03/20/98	JAPAN			ABSTRACT
		2000-349229	12/15/00	JAPAN			ABSTRACT
		05-283606	10/29/93	JAPAN			ABSTRACT

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	YODA, T. et al., "Semiconductor Integrated Circuit Device Having Interposer And Method of Manufacturing The Same", U.S. Patent Application No. 09/669,724, filed on September 26, 2000.

Examiner	Date Considered

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO 1449 — Patent and Trademark Office - U.S. Department of Commerce